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A study on design and optimization of cmos low power operational transconductance amplifier

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Abstract

Portable systems, such as wireless communication systems, laptops, smart phones, consumer electronics, and implanted medical devices, are in high demand in the rapidly expanding consumer market. When it comes to extending the running duration of these portable devices, low-power and low-voltage integrated circuits are used almost universally to achieve this. The design of an analogue integrated circuit with somewhat excellent processing characteristics, when compared to its digital equivalent, is a difficult undertaking, especially when it comes to applications requiring low voltage and low power. The use of a digitally driven CMOS technology for the design of an analogue circuit equivalent has increased the difficulty of the difficulties in today's environment. Because of this, the design of ultra-low power analogue circuits has become the bottleneck in the contemporary Complementary Metal Oxide Semiconductor (CMOS) technology. This thesis analyses some of the frequently utilised low power design strategies, which are specifically suited for analogue circuits and are being widely adopted. In today's electronic age, it is necessary to build competitive analogue integrated circuits in order to stay up with the high performance digital integrated circuits that are now available. Since its invention, the amplifier has played a critical role in the design of the vast majority of analogue integrated circuits. Despite this, the performance of the amplifier is what distinguishes the majority of analogue circuits such as converters, filters, and tracking circuits.

Keywords: *cmos, amplifier, optimization*

Introduction

With the increasing popularity of electronic devices in today's consumer market, it is driving the electronic sector to produce more energy efficient and high-performance electronic items. Especially in the fields of medical technology and wireless communication [1,2], this is true. A growing need for portable electronic devices such as mobile phones, laptops, smart watches, and hearing aids has also fueled the efforts of researchers, scientists, and academics to develop battery-powered multipurpose electronic products [3]. The use of Complementary Metal Oxide Semiconductor (CMOS) technology in the design and fabrication of modern electronic circuits not only helps to reduce the power consumption of these devices, but it also aids in the achievement of area efficiency through the use of Metal Oxide Semiconductor (MOS) scaling [4]. The CMOS devices also possess high input impedance, a high packing density, and preferably negligible static power consumption [5, as well as the ability to be rapidly and inexpensively scaled down. CMOS technological advancements, along with the availability of contemporary computer-aided design tools, raise

the likelihood of producing multifunctional, high-performance integrated circuits in the future. The widespread use of such integrated circuits in the production of low-cost portable gadgets has resulted in a significant increase in demand for them. The development of low voltage, low power integrated circuits has become more important in order to extend the life lifetime of these battery-operated portable gadgets. Currently, great effort is being put forward to meet the power demands of such low-cost portable devices by ensuring that low voltage low power designs are matched with performance that is comparable [1-5] to high-end devices. Overall, current CMOS technology is being propelled by the demand for digital CMOS circuit design, in which the use of low supply voltages is reducing the power consumption of these digital circuits in a sustainable manner [5]. Additional to this, scaling down MOS transistors results in a significant increase in the area efficiency of digital devices while having no adverse effect on their processing characteristics. A lower supply voltage, on the other hand, does not always result in a lower power usage in an analogue circuit. Furthermore, the lower supply voltage has a negative impact on the performance characteristics of analogue circuits, such as dynamic range, gain, offset, and noise [3, 4]. Sub-micron CMOS technology for the construction of a high performance, but low voltage and power, analogue circuit is a difficult undertaking that requires a great deal of expertise. Furthermore, minimum-sized transistors are incapable of assisting in the development of high-quality analogue circuits, nor are they capable of achieving considerable area reduction when compared to their digital equivalents. In order to stay up with their high-performance digital equivalents, mixed-signal integrated circuits must be designed with competitive analogue circuits that are both small in size and efficient in terms of power consumption. When it comes to analogue integrated circuit development, operation amplifiers (also known as operational transconductance amplifiers (OTA)) have played a crucial role as foundational elements since the beginning [4,6]. An increasing number of important applications, such as analogue and switching capacitor filters [2, 7-15], converters [16-21], and sigma-delta modulators [22-27], among others, are now based on the OTA architecture, including: It is the performance of this application's OTA that is mostly responsible for its overall performance. In fact, an OTA is one of the most energy-intensive components in these applications. Reduced supply voltage has a substantial influence on the ability of an OTA to handle signals effectively. Specifically, this is true when it comes to the dynamic range of an amplifier. Bottom allowed signal voltages push the top limit of the dynamic range down, whilst higher noise voltages caused by reduced supply currents bring the lower limit of the dynamic range down [28], and vice versa. It is very necessary for a low voltage amplifier to be able to cope with signal voltages that vary from rail to rail in order to have a wide dynamic range of operation. As a result, there is a need to replace the classical circuit solutions with modern layouts, which results in an increase in biassing complexity. OTAs' unity gain frequency and slew rate are both significantly affected by low-power operation [4,6,9] as well. In the event that the load capacitor is unable to be stretched to its lower limit, the bandwidth and slew rate will be significantly reduced as a result of the lower supply currents [29 - 33]. Additionally, low voltage amplifiers usually require cascaded gain stages in order to get appropriate low frequency gain [35-37]. As a result, three-frequency compensation methods become more complicated. When operating in low voltage, low power situations, it is critical that such frequency correction algorithms make excellent use of the available power [38]. All of the foregoing information motivates us to build an OTA that has strong processing characteristics while operating under a low voltage and low power limitation in a current sub-micron CMOS technology. An OTA architecture, on the other hand, is extremely important when dealing with low voltage and low power restrictions.

OTA Topology

The structure of the OTA has a significant influence on its performance characteristics. In order to achieve various goals, multiple OTA topologies have been proposed up to this point. These described topologies may be largely divided into two types, which are as follows:

- Single stage OTA
- Multi-stage OTA

Single stage OTA

In this chapter, an in-depth analysis and design aspect for many single stage OTA structures is presented. The following are some of the preliminary benefits provided by these OTAs:

1. It has a straightforward design.

The common mode signal rejection is quite high.

3. A large amount of bandwidth

4. Power usage is really low.

5. Harmonic distortion has been reduced.

6. There is a significant voltage swing.

7. Extremely fast.

Single stage OTA, on the other hand, provides a very tiny gain due to the low output impedance and bounded transconductance The downscaling of MOS Transistors (MOSTs), as a result of the lower output resistance, has also had an influence on their intrinsic gain [4,9. OTA gain enhancement approaches in the sub-micron CMOS process are summarised in Figure 1.1 and briefly described in the following sections:

Transconductance (Gm) Enhancement Enhancement of the gain of the OTA circuit can be accomplished by raising its transconductance, which is a subset of the transconductance of the input stage transistor. Amounts of transconductance can be raised in an input transistor by raising either its drain current or its aspect ratio, depending on which is greater. Either option comes at a cost in terms of power consumption, or the former limits the speed of the OTA transmission. Gain enhancement achieved by transconductance improvement is described in detail in.

Sub-threshold MOS Transistor: Applying an input voltage less than the threshold voltage operates the MOST in a sub-threshold /weak inversion region. Since very low current flows through the MOST it offers a comparatively large output resistance. In addition, MOST provides a relatively large Gm/Id efficiency. This leads to a comparatively large voltage gain. However, a very small drain current of MOST limits the slew rate of the OTA circuit [52-62].

Output resistance enhancement: Gain augmentation by the use of large output resistance is a well-developed technique that may be done through the use of methods such as positive feedback, cascoding techniques, and controlled cascoding techniques, amongst others. This approach, known as positive feedback, generates negative conductance at the output node, hence increasing the output impedance. The application of the positive feedback approach, on the other hand, severely lowers the phase margin and causes an OTA to become unstable. Comparing the cascoding approach depicted in Figure 1.2 (a), where MOST are stacked on top of one other, to the positive feedback technique, the cascoding technique gives a somewhat better phase margin while also improving resistance.

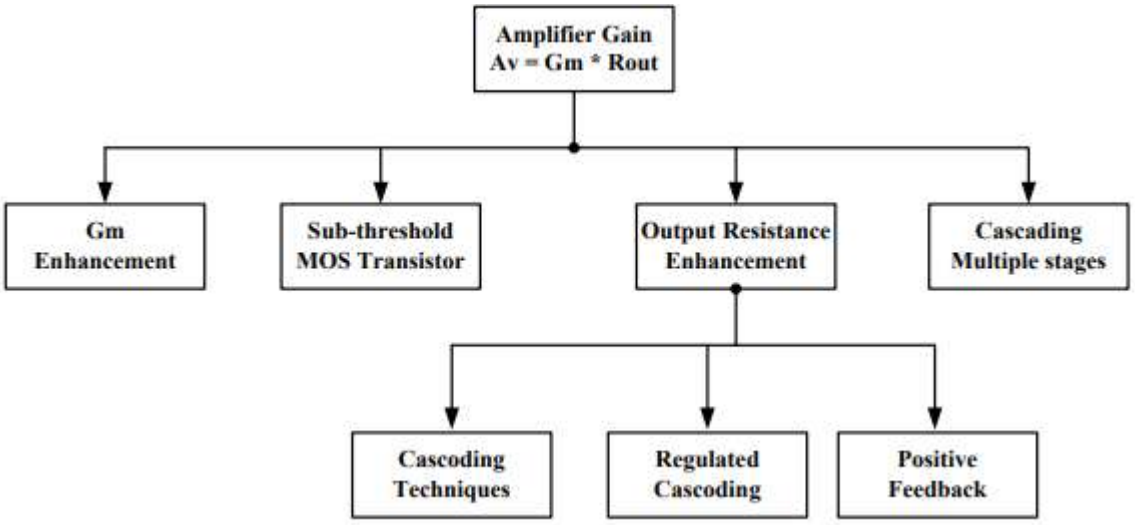

Figure 1.1. Gain enhancement techniques

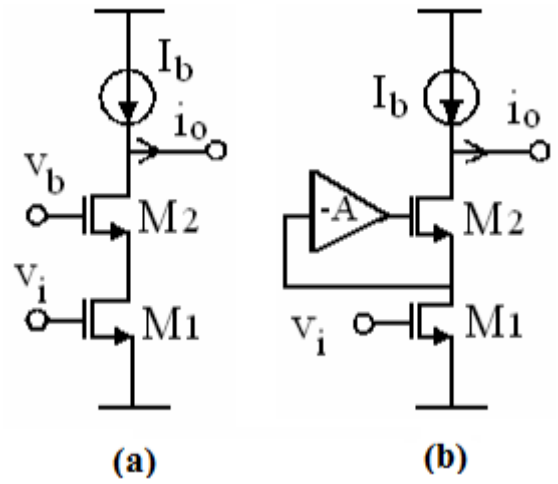

Figure 1.2. (a) cascode transconductor (b) regulated-cascode transconductor

When using the cascoding process, however, stacking transistors helps to limit the output voltage swing of the OTA. Although this is a negative, the cascoding approach is extensively used to increase the gain of OTAs since it is simple to implement and has a low power consumption structure. Using regulated cascoding, as represented in Figure 1.2 (b), it is possible to modify the standard cascoding approach even further Regulated cascoding is a technique that employs an extra auxiliary amplifier to drive the cascoding transistor. The inclusion of a second amplifier, on the other hand, makes the circuit more complicated and increases the overall power and area consumption of the OTA.

Objectives

1. Develop and implement a strategy to improve the performance of an OTA that is suited for use in a low voltage, high power environment.
2. Improving the overall performance of the proposed OTA while keeping its gain, bandwidth, slew rate, and power consumption as low as possible.
3. OTA structures should be designed and simulated in order to confirm their performance utilising currently available sub-micron CMOS technology.

Methodology

In order to address any concerns that may arise as a result of the study, practical research aspects such as power consumption, gain, bandwidth, slew rate, and noise performance will be incorporated into the study.

Aims of the research include developing an analytical or descriptive solution to improve the performance of existing OTAs, as well as preparing an experimental set to attain the same goal. Among the aspects of the research are the examination of modern Electronics Design Automation (EDA) tools such as Cadence Design Suit and Win-Spice, which are required for validating the performance of the proposed as well as previously reported OTA topologies using the currently available sub-micron CMOS technology. A secondary goal of this research is to investigate the influence of process, voltage, and temperature variations on the performance of the proposed optical transducer.

Result

In order to illustrate the performance improvement of the PRFC OTA, the traditional FC, the RFC, and the PRFC OTA structures are developed and implemented in standard 180nm CMOS technology to demonstrate the performance improvement of the PRFC OTA. All transistors are biassed in the weak inversion region in order to achieve low power consumption, and the complete circuit is run with a supply voltage of 0.5V in order to achieve this. A biassing current of 5uA has been established. OTA structure construction and simulation are carried out in a Cadence Design Suit environment, which is called the Analog Design Environment (ADE). The simulated open loop AC response of the FC, the RFC, and the PRFC OTA for a load capacitor of CL=20pF and a biassing current of 5uA is depicted in Figure 1.3 for the FC, the RFC, and the PRFC OTA. As seen in Figure 1.3, the PRFC OTA exhibits about 13dB and 8.5dB greater gains when compared to the FC and RFC OTAs, respectively, compared to the FC and RFC OTAs. It is discovered that the PRFC OTA has a ground beam width of 224.10 KHz, whereas the FC and RFC OTAs have ground beam widths of 40.78 KHz and 122.94 KHz, respectively (see Figure 1). When

compared to the FC and RFC OTAs, the PRFC OTA displays an approximate improvement in the GBW of 450 percent and 90 percent, respectively, as a result of the transconductance enhancement. In terms of measured PMs at their respective ground-breaking weights (GBW), the FC, the RFC, and the PRFC OTA have measured 87.78, 87.12, and 79.52, respectively. The use of a positive feedback circuit causes the PM of the PRFC OTA to decline, but it keeps the PM above the 750 mark. In spite of the increased GBW and DC gain, the PRFC OTA exhibits excellent stability. Figure 4.8 depicts the OTA behaviour of the RFC and the PRFC when dealing with big signals. Slewing motion in both OTAs is generated by applying a big step signal of 300mV and 50 kHz to the OTAs. The average slew rate for the RFC and the PRFC OTA is 136.9 V/ms and 202.4 V/ms, respectively, for the RFC and the PRFC, respectively. As seen in Figure 1.4, there is no ringing effect detected. Positive feedback has a minor influence on the phase margin, as seen by this example. It takes 28.58us and 24.09us, respectively, for the RFC and the PRFC OTA to reach a one percent settling time (ST). an influence on key performance characteristics of the PRFC OTA. If we look at we can see that the FF corner exhibits an estimated improvement of 500 and 4000 percent in GBW, respectively, in comparison to the TT and S corners, with a minimal decrease in the PM. In a similar vein, the average slew rate seen for the FF corner is six times greater than that observed for the TT corner and sixty-five times higher than that observed for the SS corner.

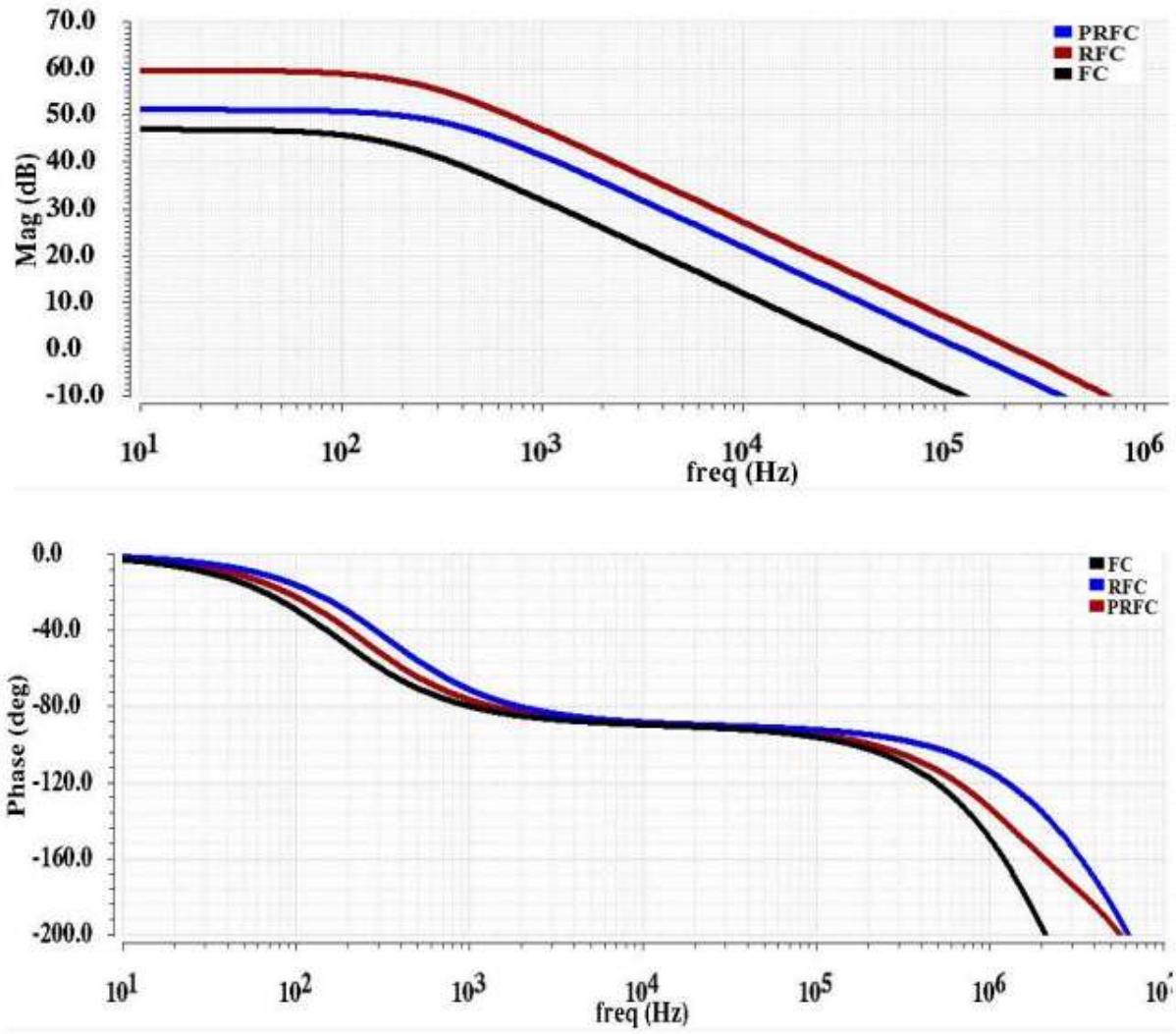

Figure 1.3. AC response of FC, RFC and PRFC OTA

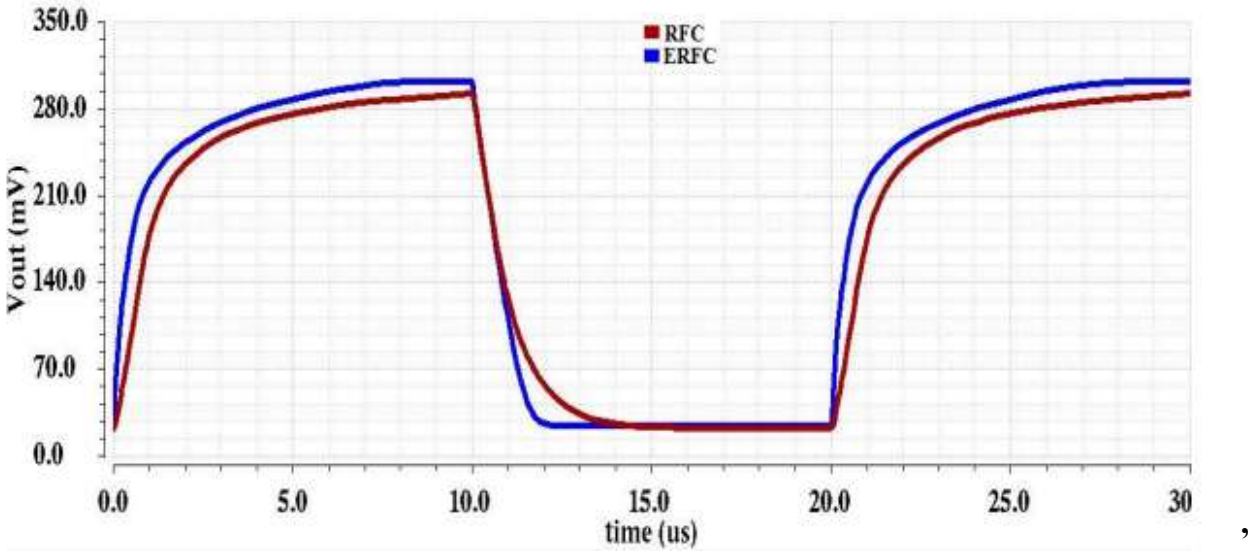

Figure 1.4 Large signal behavior of RFC and PRFC OTA

Conclusion

Despite this, the amplifier design is customized to the application. The amplifier's bandwidth, gain, offset, slew rate, and noise, on the other hand, are likely the most important design factors to consider. When it comes to developing a low voltage, low power application, the OTA topology is critical to consider. Despite the fact that multistage amplifiers have advantages such as higher gain, more rail-to-rail output voltage swing, and better noise tolerance, they are still unable to match the speed and power efficiency of single stage structures. According to the results of the above study, the RFC OTA uses only half the power of the Telescopic and FC OTAs while performing similarly well, making it the best ideal for low voltage, low power applications. It is mostly based on design criteria like as bandwidth, speed, offset, noise, and circuit complexity that are application specific when deciding on a low voltage low power method. The addition of asymmetrical current splitting to the RFC OTA's input stage results in a considerable improvement in the overall performance of the RFC OTA. Without impacting the current RFC OTA circuit's power budget, the upgrade has been accomplished. GBW and DC gain were increased by 520 percent and 13.7 decibels, respectively, above the baseline of the typical FC OTA, according to the measurement results, which verifies the transconductance augmentation. Additionally, the simulation results demonstrate that the suggested OTA has the capability of operating as a tunable OTA merely by altering the voltage source.

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